Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

1. Revision Record

REV NO.	REV DATE	CONTENTS	Note
A	2015-09-25	NEW ISSUE	

2. Table of Contents

3. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.
If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

4. PRODUCT INFORMATION

4.1. Description

DBT040TS02A is a color active matrix LCD module incorporating amorphous silicon TFT(Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 4.0″ display area contains 480(RGB) x 800pixels and can display up to 16.7M colors.

4.2. Applications

UMPC
Digital photo frame
GPS

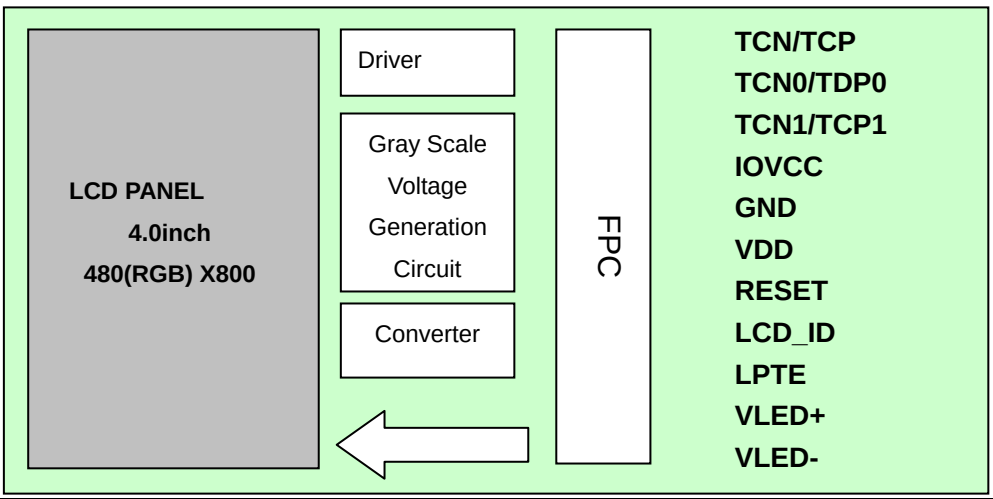
4.3. Features

High Resolution: 480(RGB) x 800 Dots
Panel Size:4.0(16:9 diagonal) inch
Interface: MIPI
8 LED backlight

4.4. General Specifications

Item	Specification	Unit	Remark
Display Mode	Normally Black	-	-
Outline Dimension	57.14(H) X 96.85(V) X2.05(T)	mm	-
Active Area	51.84(H) x86.40 (V)	mm	-
Resolution	480X(RGB)X800	dots	-
Pixel Pitch	108X108	μm	-
Pixel Configuration	RGB Stripe	-	-
Weight	TBD	g	-
Luminance	400（TYP）	cd/m2	-
Signal Interface	MIPI	-	-
Viewing Direction	Free	o'clock	Note

4.5. <Block diagram>



5. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit
Logic supply voltage	VDD3	Ta= 25℃	-0.3	4.6	V
Supply voltage for step-up circuit	VCI	Ta= 25℃	-0.3	4.6	V
LCD supply voltage range	|VGH-VGL|	Ta= 25℃	-0.3	32	V
Operating temperature	Topa	Ta= 25℃	-20	65	℃
Storage temperature	Tstg	Ta= 25℃	-40	85	℃
Storage humidity	Hstg	Ta= 25℃	10	90	%

Note:

*1) If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop. It is not allowed for any of these ratings to be exceeded. Make sure all the design characteristics are adequate before the panel is initialed.

*2) All the measurements should be operated with driver IC and experimental FPC mounted.

6. ELECTRICAL SPECIFICATIONS(Ta=25°C)

6.1. DC CHARACTERISTICS

Recommend Parameters for Electrical Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Remark
Input power supply		VDD3	V	1.65	1.8	3.3	Note 1
		VCI	V	2.5	2.8	3.3	
Current Spec	MIPI I/F	Idd+Ici	mA	-	-	35	Note 2
		Islp	uA	-	-	250	-
	RGB I/F	Idd+Ici	mA	-	-	35	-
		Islp	uA	-	-	150	-
Frame	MIPI I/F RGB I/F	Hz		-	60	70	Note 3
Input Signal Voltage	H Level	VIH	V	0.7 x VDD3	-	VDD3	-
	L Level	VIL	V	0	-	0.3 x VDD3	
Output signal Voltage	H Level	VOH	V	0.8 x VDD3	-	VDD3	-
	L Level	VOL	V	0	-	0.2 x VDD3	
LDI ESD		HBM	kV	-2	-	+2	-
		MM	V	-200	-	+200	

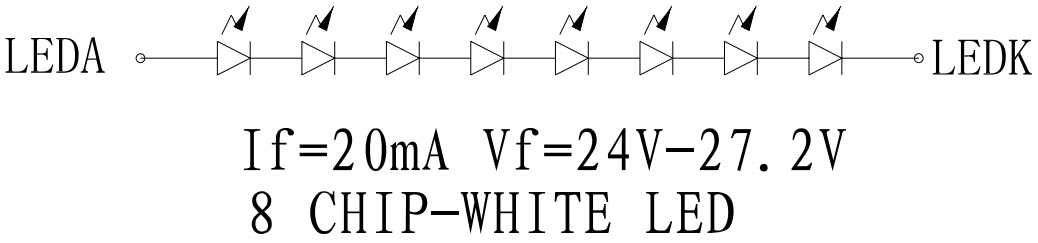
Note:

*1) The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during operation. To prevent noise, a bypass capacitor must be inserted into the line close to power pin. Please make sure all the design settings are used within this range before the panel is initialed

*2) Please make sure that DC is not supplied to LCD for long period. And do not supply voltage to LCD while within "sleep mode".

*3) All the measurements should be operated with driver IC and experimental FPC.

6.2. Backlight Driving Section



6.3. BACKLIGHT CHARACTERISTICS

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage	VF	24	25.6	27.2	V	-
LED Forward Current	IF	-	20		mA	-
Operating LED life time	Hr	20000	40000		Hour	(1)

Remarks (1) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IF=240mA.

7. OPTICAL SPECIFICATIONS(Ta=25℃)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Threshold Voltage		Vsat	4.1	4.3	4.5	V	
		Vth	1.6	1.8	2.0	V	
Contrast Ratio		C/R	650	900	1300		Fig.1
Brightness		-	350	400	-	cd/m2	Full White Pattern (Transmittance 7.4%)
NTSC		%	65%	70%	75%		
Brightness Uniformity			80	-	-	%	Full White Pattern
Response Time		Tr+Tf	-	35	42	ms	Fig.3
Color Coordinate	WHITE	Wx	0.268	0.288	0.308		IBL=20mA Full White Pattern
		Wy	0.299	0.319	0.339		
view angle		θl	70	85	-	Degree	Fig.4 Center (C/R>10)
		θr	70	85	-		
		θu	70	85	-		
		θd	70	85	-		

Note:

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

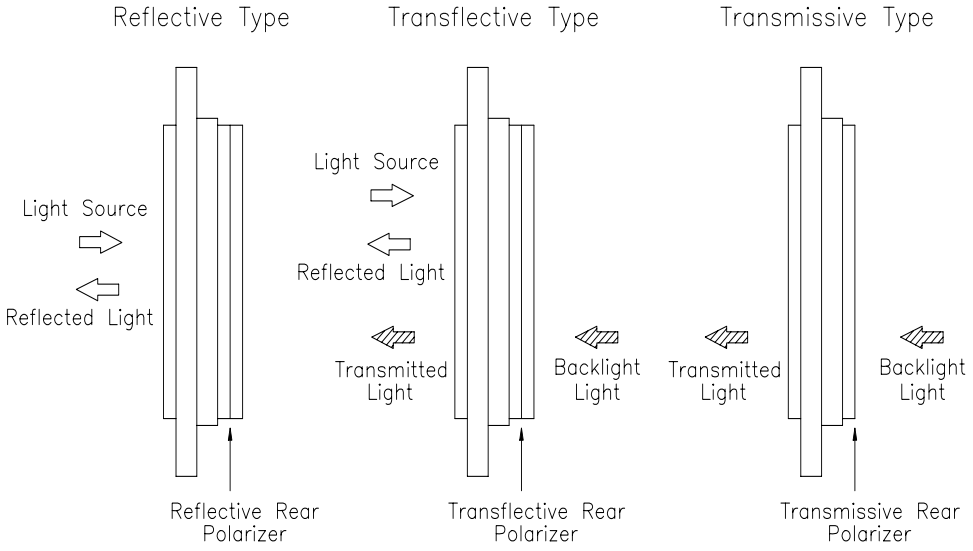
2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.

3. Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf). For additional information see FIG 3.

4. Viewing angle is the angle at which the contrast ratio is greater than 5. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

5. Optimum contrast is obtained by adjusting the LCD Threshold voltage (Vth& Vsat)

8. Viewing Modes



9. Electro-Optical Characteristics Test Method

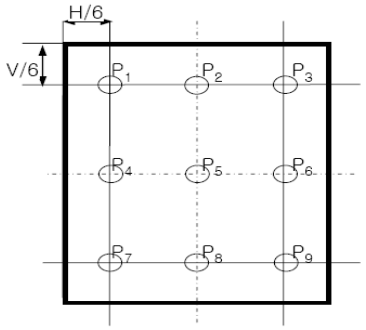


Fig. 2 Measuring Points

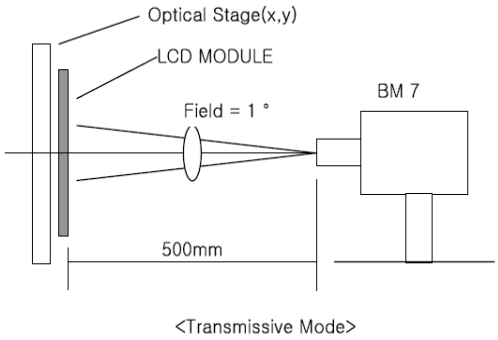


FIG. 1 Optical Characteristic Measurement Equipment and Method

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

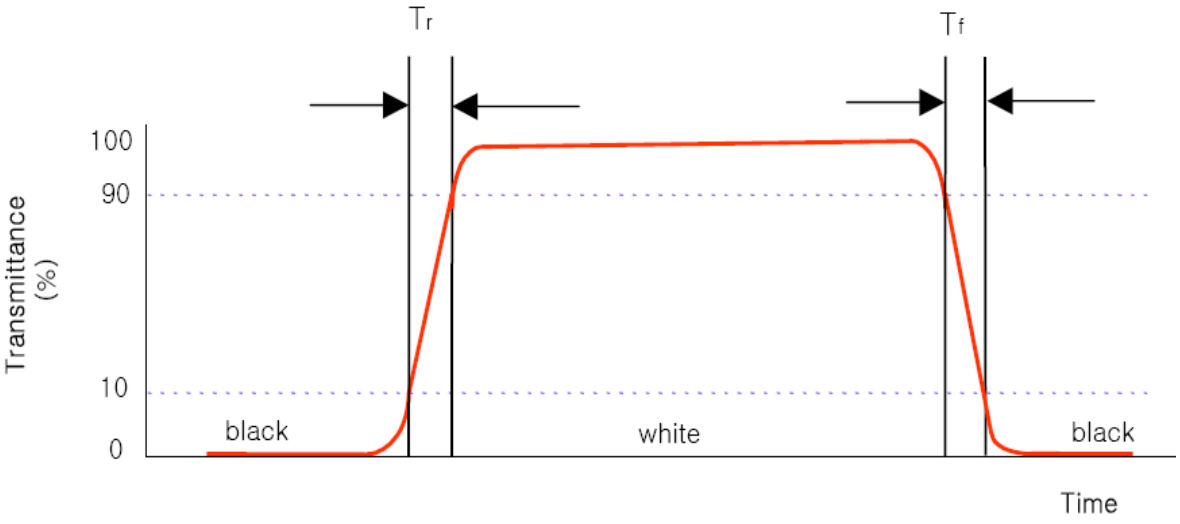


FIG.3 The definition of Response Time

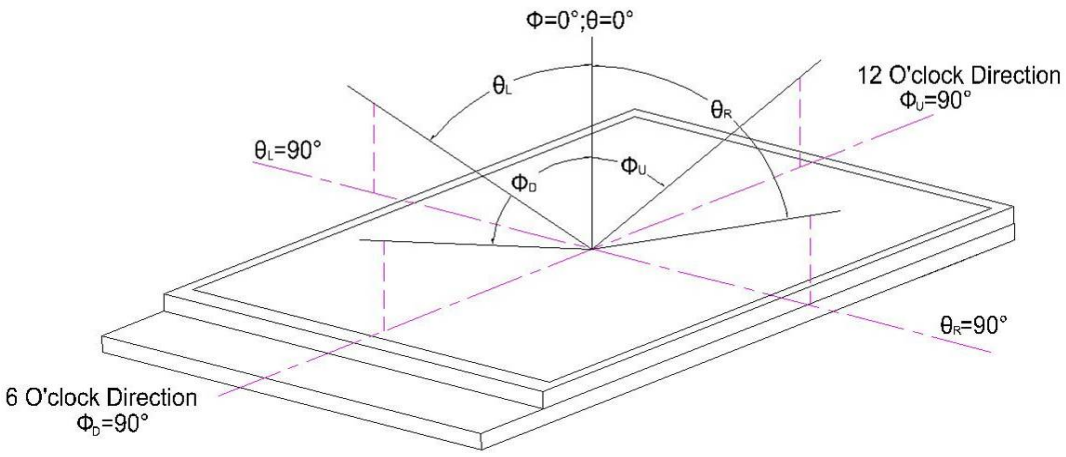
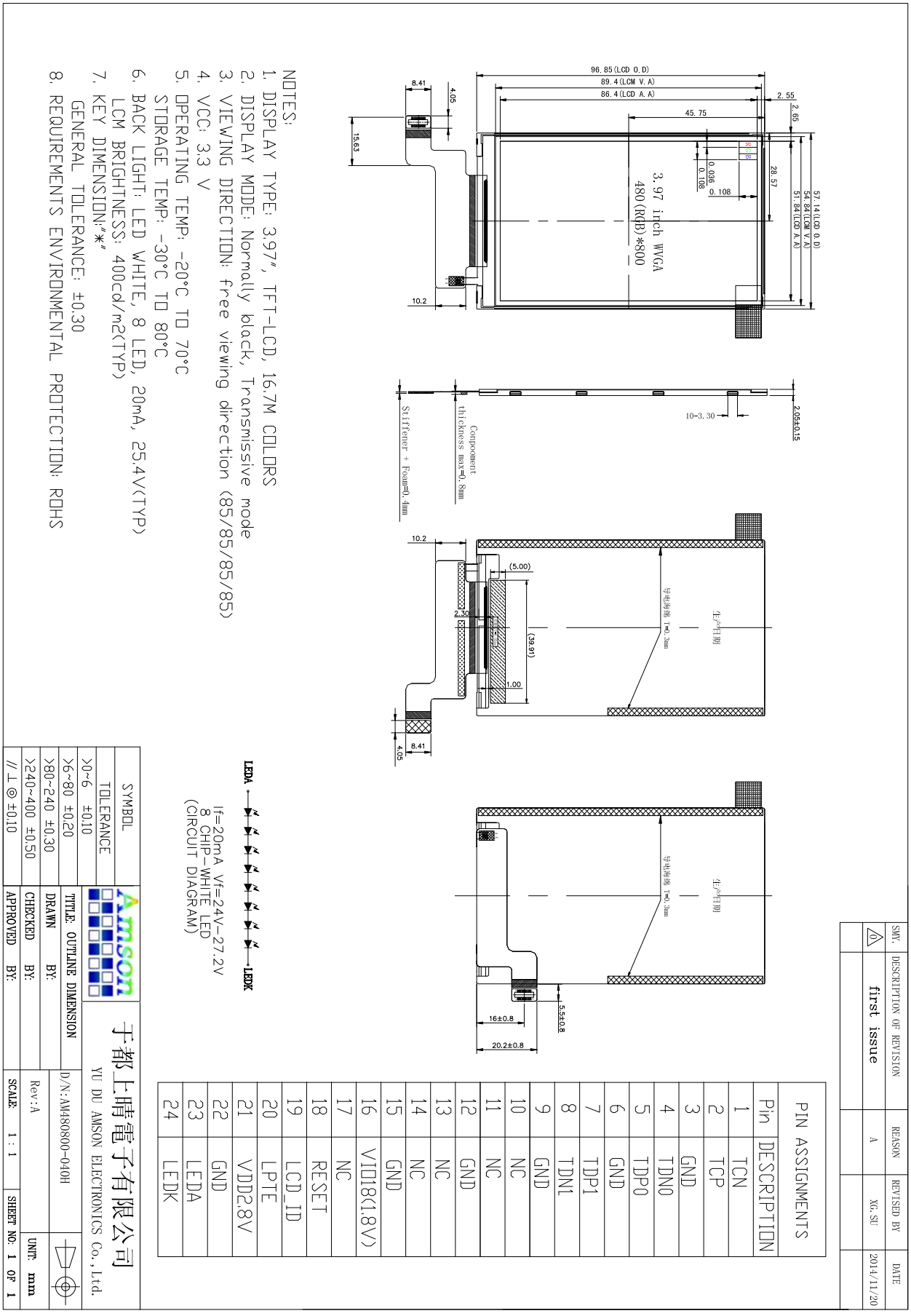


FIG.4 The definition of Viewing Angle

10. Outline dimension



SYMBOL	TOLERANCE
>0~6	±0.10
>6~80	±0.20
>80~240	±0.30
>240~400	±0.50
// ⊥ ◎	±0.10

SMY.	DESCRIPTION OF REVISION	REASON	REVISED BY	DATE
	first issue	A	XG. SU	2014/11/20

PIN ASSIGNMENTS

Pin	DESCRIPTION
1	TCN
2	TCP
3	GND
4	TDN0
5	TDP0
6	GND
7	TDP1
8	TDN1
9	GND
10	NC
11	NC
12	GND
13	NC
14	NC
15	GND
16	VDD18(1.8V)
17	NC
18	RESET
19	LCD_ID
20	LPTE
21	VDD2.8V
22	GND
23	LEDA
24	LEDK

Amson
于都上晴電子有限公司
YU DU AMSON ELECTRONICS Co., Ltd.

TITLE: OUTLINE DIMENSION		D/N:AM480800-040H
DRAWN BY:		Rev:A
CHECKED BY:		UNIT: mm
APPROVED BY:	SCALE: 1 : 1	SHEET NO: 1 OF 1

11. Table of Pin Assignment

LCM Pin Assignment

Pin No.	Symbol	I/O	Description	Remark
1	TCN	I	MIPI-DSI Clock Lane Negative	
2	TCP	I	MIPI-DSI Clock Lane Positive	
3	GND	P	ground	
4	TDN0	I	MIPI-DSI Data Lane Negative 0	
5	TDP0	I	MIPI-DSI Data Lane Positive 0	
6	GND	P	ground	
7	TDN1	I	MIPI-DSI Data Lane Negative 1	
8	TDP1	I	MIPI-DSI Data Lane Positive 1	
9	GND	P	ground	
10	NC	-	No Connect	
11	NC	-	No Connect	
12	GND	P	ground	
13	NC	-	No Connect	
14	NC	-	No Connect	
15	GND	P	ground	
16	VDDIO	I	I/O PWOER	
17	NC	I	No Connect	
18	RESET	I	RESET Signal	
19	LCD_ID	I	LCD_ID	
20	LPTE	O	Tearing effect output pin	
21	VDD2.8V	I	Power Supply	
22	GND	P	ground	
23	LEDA	I	LABAR Positive	
24	LEDK	I	LABAR Negative	

Note 1: I/O---Input/Output; I---Input; P---Power/Ground

12. MIPI-DSI interface

12.1. General description

The communication can be separated 2 different levels between the MCU and the display module

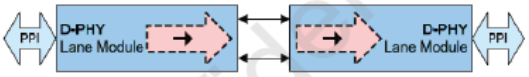
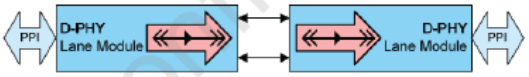
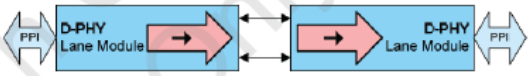
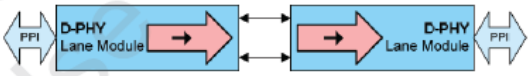
-Interface Level: Low level communication

-Packet level: High level communication

12.2. Interface level communication

12.3.General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can driven Low Power(LP)or High Speed(HS)mode. Data lane1 and Data lane2 can be driven High speed mode only.

	Lane support mode	MPU(Host) OTM8009A(Slave)
Clock Lane	Unidirectional lane ★High-Speed Clock only ★Simplified Escape Mode (ULPS Only)	
Data lane0	Bi-directional lane ★Forward high-speed only ★Bi-directional Escape Mode ★Bi-direction LPDT	
Data lane1	Unidirectional lane ★Forward high-speed only ★Simplified Escape Mode (ULPS Only)	
Data lane2	Unidirectional lane ★Forward high-speed only ★Simplified Escape Mode (ULPS Only)	

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable)and it can be driven into a low power mode.

High Speed mode means that different modes and protocols in each mode when there are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The state Codes of the High Speed (HS)and Low Power(LP)lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

13. Reliability

Item NO.	Test Item	Test condition	Description
1	**High temperature operation**	**Ta=70℃,240 h**	**Endurance test applying the electric operation under high temperature for a long time**
2	**Low temperature operation**	**Ta=-20℃,240 h**	**Endurance test applying the electric operation under low temperature for a long time**
3	**High temperature storage**	**Ta=80℃,240 h**	**Endurance test applying the high storage temperature for a long time**
4	**Low temperature storage**	**Ta=-30℃,240 h**	**Endurance test applying the low storage temperature for a long time**
5	**High temperature High humidity**	**Ta=60℃, 90%RH,240 h**	**Endurance test applying electric operation under high temperature and high humidity for a long time**
6	**Temperature Cycle**	**-30℃(30min), +80℃(30min) 200cycles**	**Endurance test applying the low and high temperature cycle** **One cycle**
7	**Shock Test**	**100G ,6ms Direction: X,Y,Z 3 times**	**Measure an aerospace product's response to mechanical shock**

14. packaging

TBD